In the Claims

1   1. A method of identifying faulty programmable interconnect
2 resources of a field programmable gate array during normal on-line operation
3 comprising the steps of:
4   configuring said field programmable gate array into a self-
5 testing area and a working area, said working area maintaining normal
6 operation of the field programmable gate array;
7   testing programmable interconnect resources located within
8 said self-testing area for faults;
9   identifying at least one programmable interconnect resource
10 having a fault detected during said testing step.

1   2. The method set forth in Claim 1, wherein the step of testing
2 said programmable interconnect resources located within said initial self-
3 testing area for faults includes propagating test patterns along at least two
4 groups of wires under test;
5   comparing outputs of said at least two groups of wires under
6 test; and

7   producing fault status data for said at least two groups of wires

8   under test.

1   3. The method of identifying faulty programmable interconnect

2   resources set forth in claim 2, wherein said identifying step includes

3   minimizing a region of one of said groups of wires under test which includes

4   said fault.

1   4.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 3, wherein said identifying step

3   includes reconfiguring said minimized region of said group of wires under

4   test for further testing in order to identify a wire within said minimized region

5   which includes said fault.

1   5.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 4, wherein said identifying step

3   includes replacing programmable interconnect resources within said wire for

4   further testing in order to identify a wire segment, a configuration

5   interconnect point, and/or a combination thereof which includes said fault.

1   6.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 2, wherein said identifying step

3   includes reconfiguring said groups of wires under test for further testing in

4   order to identify a wire within said groups of wires under test which includes

5   said fault.

1   7.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 6, wherein said identifying step

3   includes minimizing a region of said wire which includes said fault.

1   8.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 7, wherein said identifying step

3   includes replacing programmable interconnect resources within said

4   minimized region of said wire for further testing in order to identify a wire

5   segment, a configuration interconnect point, and/or a combination thereof

6   which includes said fault.

1   9. A method of identifying faulty programmable interconnect

2   resources of a field programmable gate array during normal on-line operation

3   comprising the steps of:

4   configuring said field programmable gate array into a self-

5   testing area and a working area, said working area maintaining normal

6   operation of the field programmable gate array;

7   testing groups of programmable interconnect resources located

8   within said self-testing area for faulty resources;

9   minimizing a region of at least one of said groups of

10   programmable interconnect resources determined to include said faulty

11   resource;

12   reconfiguring said region for further testing in order to identify

13   said faulty resource detected during said initial testing step; and

14   repeating the steps of reconfiguring and testing until said faulty

15   resource is identified.

1   10.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 9, wherein said self-testing area

3   includes programmable logic blocks configured to function as at least one

4   test pattern generator and at least one output response analyzer, and

5   programmable interconnect resources configured as at least two groups of

6   wires under test.

1   11.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 10, wherein the step of testing said

3   groups of programmable interconnect resources includes propagating test

4   patterns generated by said at least one test pattern generator along said at

5   least two groups of wires under test, comparing outputs of said at least two

6   groups of wires under test using said at least one output response analyzer,

7   and producing fault status data for said at least two groups of wires under

8   test.

1   12.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 11, wherein the step of testing said

3   groups of programmable interconnect resources includes comparing the

4   outputs of said at least two groups of wires under test with an output of at

5   least one additional group of wires under test in order to determine which of

6   said at least two groups of wires under test includes said faulty resource

7   detected during said initial testing step.

1   13.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 12, wherein the step of minimizing

3   a region of said at least one group of programmable interconnect resources

4   determined to include said faulty resource includes establishing said

5   interconnect resources located within said self-testing area as at least two

6   subsequent groups of wires under test, at least one of said subsequent groups

7   including a subdivided portion of said resources located within said faulty

8   group of wires under test; and

9   testing resources located within said subsequent groups of

10   wires under test for faults in order to determine which subsequent group of

11   wires under test includes said faulty resource.

1   14.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 13, wherein the steps of establishing

3   and testing are repeated until the region of said group of wires under test

4   which includes said faulty resource is minimized.

1   15.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 14, wherein the step of reconfiguring

3   said region includes re-routing programmable interconnect resources within

4   said minimized region to avoid suspect resources for further testing in order

5   to identify a wire segment, a configuration interconnect point, and/or a

6   combination thereof which includes said fault.

1   16.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 9, further comprising the step of

3   roving said self-testing area by reconfiguring the field programmable gate

4   array such that a portion of the working area becomes a subsequent self-

5   testing area and at least a portion of the initial self-testing area becomes a

6   portion of the working area.

1   17.   An apparatus for identifying faulty programmable

2   interconnect resources of a field programmable gate array comprising:

3   a controller in communication with the field programmable gate

4   array for: (a) configuring the field programmable gate array into a self-

5   testing area and a working area, the working area maintaining normal

6   operation of the field programmable gate array; (b) initiating testing of

7   groups of programmable interconnect resources located within the self-

8   testing area for faults; (c) reconfiguring groups of resources determined to

9   include a faulty resource for further testing in order to minimize a region of

10   the group of resources which includes the faulty resource; (d) repeating the

11   steps of testing and reconfiguring until the region of the group of resources

12   which include the faulty resource is minimized; (e) reconfiguring the

13   resources located within the minimized faulty region of the group of

14   resources for further testing in order to identify the faulty resource by re-

15   routing portions of the minimized faulty region to avoid suspect resources;

16   and (f) repeating the steps of reconfiguring and further testing until the faulty

17   resource is identified.

1   18.   The apparatus for identifying faulty programmable

2   interconnect resources of a field programmable gate array of claim 17, further

3   comprising a storage medium in communication with said controller for

4   storing a functional configuration of the field programmable gate array, a

5   plurality of test configurations, and fault status data.

1   19.   The apparatus for identifying faulty programmable

2   interconnect resources of a field programmable gate array of claim 18,

3   wherein said self-testing area includes programmable logic blocks configured

4   to function as at least one test pattern generator and at least one output

5   response analyzer, and programmable interconnect resources configured as

6   at least two groups of wires under test; and

7   wherein test patterns generated by said at least one test pattern

8   generator are propagated along said at least two groups of wires under test,

9   outputs of said at least two groups of wires under test are compared using

10 said at least one output response analyzer, and fault status data for said at

11 least two groups of wires under test is produced.

1   20.   The apparatus for identifying faulty programmable

2   interconnect resources of a field programmable gate array of claim 17,

3   wherein said self-testing area roves by reconfiguring the field programmable

4   gate array such that a portion of the working area becomes a subsequent self-

5   testing area and at least a portion of the initial self-testing area becomes a

6   portion of the working area.

1   21. A method of identifying faulty programmable interconnect

2   resources of a field programmable gate array comprising the steps of:

3   configuring programmable logic blocks of said field

4   programmable gate array to function as at least one test pattern generator and

5   at least one output response analyzer, and programmable interconnect

6   resources as at least two groups of wires under test;

7   testing said at least two groups of wires under test faults;

8   identifying at least one programmable interconnect resource

9   having a fault detected during said testing step.

1   22.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 21, wherein the step of testing said

3   at least two groups of wires under test for faults includes propagating test

4   patterns along said least two groups of wires under test;

5   comparing outputs of said at least two groups of wires under

6   test; and

7   producing fault status data for said at least two groups of wires

8   under test.

1   23.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 22, wherein said identifying step

3   includes minimizing a region of one of said groups of wires under test which

4   includes said fault.

1   24.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 23, wherein said identifying step

3   includes reconfiguring said minimized region of said group of wires under

4   test for further testing in order to identify a wire within said minimized region

5   which includes said fault.

1   25.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 24, wherein said identifying step

3   includes replacing programmable interconnect resources within said wire for

4   further testing in order to identify a wire segment, a configuration

5   interconnect point, and/or a combination thereof which includes said fault.

1   26.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 22, wherein said identifying step

3   includes reconfiguring said groups of wires under test for further testing in

4   order to identify a wire within said groups of wires under test which includes

5   said fault.

1   27.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 26, wherein said identifying step

3   includes minimizing a region of said wire which includes said fault.

1   28.   The method of identifying faulty programmable

2   interconnect resources set forth in claim 27, wherein said identifying step

3   includes replacing programmable interconnect resources within said

4   minimized region of said wire for further testing in order to identify a wire

5   segment, a configuration interconnect point, and/or a combination thereof

6   which includes said fault.